

ANNA UNIVERSITY COIMBATORE

**FACULTY OF
ELECTRONICS & COMMUNICATION
ENGINEERING**

BOARD OF STUDIES -ECE

M.E. VLSI DESIGN

CURRICULUM AND SYLLABI

I –IV SEMESTERS

REGULATIONS - 2007

ANNA UNIVERSITY: COIMBATORE
M.E. VLSI DESIGN
CURRICULUM 2007 - FULL TIME MODE
SEMESTER – I

Code No.	Course Title	L	T	P	M
Theory					
	Applied Mathematics	3	1	0	100
	Digital Signal Processing Integrated Circuits	3	1	0	100
	Advanced Digital System Design	3	1	0	100
	VLSI Design Techniques	3	1	0	100
	Solid State Device Modeling and Simulation	3	0	0	100
	Testing of VLSI Circuits	3	0	0	100
Practical					
	VLSI Design Lab I	0	0	4	100
	Total	18	4	4	-

SEMESTER – II

Code No.	Course Title	L	T	P	M
Theory					
	Analysis and Design of Analog Integrated Circuits	3	1	0	100
	Computer Aided Design of VLSI Circuits	3	1	0	100
	VLSI Signal Processing	3	1	0	100
	Elective I	3	1	0	100
	Elective II	3	0	0	100
	Elective III	3	0	0	100
Practical					
	VLSI Design Lab II	0	0	4	100
	Total	18	4	4	-

SEMESTER – III

Code No.	Course Title	L	T	P	M
Theory					
	Elective IV	3	0	0	100
	Elective V	3	0	0	100
	Elective VI	3	0	0	100
Practical					
	Project Work (Phase I)	0	0	12	200
	Total	9	0	12	-

SEMESTER – IV

Code No.	Course Title	L	T	P	M
	Project Work (Phase II)	0	0	24	400
	Total	0	0	24	-

LIST OF ELECTIVES
M.E. VLSI DESIGN
SEMESTER II

Code No.	Course Title	L	T	P	M
	Low Power VLSI Design	3	0	0	100
	CMOS VLSI Design	3	0	0	100
	Analog VLSI Design	3	0	0	100
	Design of Semiconductor Memories	3	0	0	100
	VLSI Technology	3	0	0	100
	Physical Design of VLSI Circuits	3	0	0	100
	Genetic Algorithms and their Applications	3	0	0	100
	Advanced Microprocessors and Microcontrollers	3	0	0	100
	Neural Networks and Applications	3	0	0	100

LIST OF ELECTIVES
M.E. VLSI DESIGN
SEMESTER III

Code No.	Course Title	L	T	P	M
	ASIC Design	3	0	0	100
	Reliability Engineering	3	0	0	100
	Electromagnetic Interference and Compatibility in System Design	3	0	0	100
	DSP Processor Architecture and Programming	3	0	0	100
	Data Converters	3	0	0	100
	RF IC Design	3	0	0	100
	Analysis and Design of Digital Integrated Circuits	3	0	0	100
	Computer Architecture and Parallel Processing	3	0	0	100
	Embedded Systems	3	0	0	100
	RF MEMS	3	0	0	100
	Special Elective	3	0	0	100

SEMESTER I

07VL101 APPLIED MATHEMATICS

3 1 0 100

LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS

9+3

System of equations- Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method- Jacobi, Gauss-Seidal iteration method- Eigen values of a matrix by Jacobi and Power method.

WAVE EQUATION

9+3

Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

SPECIAL FUNCTIONS

9+3

Bessel's equation - Bessel Functions- Legendre's equation - Legendre polynomials -Rodrigue's formula - Recurrence relations- generating functions and orthogonal property for Bessel functions - Legendre polynomials.

RANDOM VARIABLES

9+3

One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient - Functions of Two dimensional random variable

QUEUEING THEORY

9+3

Single and Multiple server Markovian queueing models - Steady state system size probabilities – Little's formula - Priority queues - M/G/1 queueing system – P.K. formula.

L + T = 45 + 15 = 60

REFERENCES:

1. Sankara Rao.K. "Introduction to Partial Differential Equation ", PHI, 1995.
2. Taha. H.A., "Operations Research- An Introduction " 6th Edition, PHI, 1997.
3. Jain M.K. Iyengar, S.R.K. & Jain R.K., "International Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publishers 2003..
4. Kanpur J.N. & Saxena. H.C. "Mathematical Statistics", S.Chand & Co., New Delhi, 2003.
5. Greweal B.S. "Higher Engineering Mathematics", Khanna Publishers, 2005.

07VL102 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS

3 1 0 100

UNIT I

9

DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II **9**
DIGITAL SIGNAL PROCESSING

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III **9**
DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV **9**
DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V **9**
ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN

Conventional number system, Redundant Number system, Residue Number System .Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies

L : 45, T:15 Total 60

REFERENCES:

1. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York 1999.
2. A.V.Oppenheim et.al, ‘Discrete-time Signal Processing’ Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, “Digital signal processing – A practical approach”, Second edition, Pearson education, Asia 2001.
4. Keshab K.Parhi, ‘VLSI digital Signal Processing Systems design and Implementation’ John Wiley & Sons, 1999.
5. Bayoumi & Magdy A., “ VLSI Design Methodologies for Digital Signal Processing Architectures”, BS Publications, 2005.

07VL103 ADVANCED DIGITAL SYSTEM DESIGN **3 1 0 100**

UNIT I **9**
SEQUENTIAL CIRCUIT DESIGN

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

UNIT II **9**
ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential

Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III

9

FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault Table Method – Path Sensitization Method – Boolean Difference Method – D Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV

9

SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL – Realization State machine using PLD –Complex Programmable Logic Devices (CPLDs) - FPGA – Xilinx FPGA – Xilinx 3000 - Xilinx 4000

UNIT V

9

SYSTEM DESIGN USING VHDL

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

L :45 T:15 Total 60

REFERENCES:

1. Nelson V.P., Nagale H.T., Carroll B.D., and Irwin J.D., "Digital Logic Circuit Analysis and Design", Prentice Hall International Inc.1995.
2. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001.
3. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
4. Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Design" Tata McGraw Hill, 2002.
5. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International, 1998.
6. Parag K Lala, "Digital System design using PLD" BS Publications, 2003.
7. Parag K Lala, " Digital Circuit Testing and Testability" Academic Press, 1997.
8. Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004.
9. Dueck R.K., "Digital Design with CPLD applications and VHDL" Thomson Delmer Learning, 2001.
10. Donald G. Givone "Digital principles and Design" Tata McGraw Hill,2002.
11. Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
12. John M Yarbrough "Digital Logic applications and Design" Thomson Learning, 2001.
13. Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India Pvt Ltd, 2002.

07VL104 VLSI DESIGN TECHNIQUES

3 1 0 100

UNIT I

VLSI DESIGN PROCESS.

9

VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semicustom approaches.

MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY.

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II

9

INVERTERS AND LOGIC GATES.

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III 9

CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV 9

VLSI SYSTEM COMPONENTS CIRCUITS

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers

UNIT V 9

VERILOG HARDWARE DESCRIPTION LANGUAGE

Overview of digital design with Verilog HDL, hierarchical modelling concepts, modules and port definitions, gate level modelling, data flow modelling, behavioral modelling, task & functions, Test Bench.

L :45 T:15 Total 60

REFERENCES:

1. Jan M Rabaey, “ Digital Integrated Circuits” Prentice Hall of India, 2002
2. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis and Design”,Tata McGraw Hill,2003.
3. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
4. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
5. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004.
6. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
7. J.Bhasker, B.S.Publications, “A Verilog HDL Primer”, 2nd Edition, 2001.
8. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.
9. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education.2002.

07VL105 SOLID STATE DEVICE MODELING AND SIMULATION 3 0 0 100

UNIT I 9

BASIC SEMICONDUCTOR PHYSICS

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources.

Diodes : Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions – Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode – Temperature and Area effects on Diode Model Parameters.

UNIT II 9

BIPOLAR DEVICE MODELING

Transistor Models: BJT – Transistor Action – Minority carrier distribution and Terminal currents - Switching- Eber - Molls and Gummel Poon Model, SPICE modeling - temperature and area effects.

UNIT III 9

MOSFET MODELING

MOS Transistor – NMOS, PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV **9**
PARAMETER MEASUREMENT

Bipolar Junction Transistor Parameter – Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

UNIT V **9**
OPTOELECTRONIC DEVICE MODELING

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photodetectors.

Total: 45

REFERENCES:

1. Ben.G.Streetman, "Solid State Devices", Prentice Hall , 1997.
2. Giuseppe Massobrio and Paolo Antognetti, "Semiconductor Device Modeling with SPICE" Second Edition, McGraw-Hill Inc, New York, 1993.
3. Tyagi M.S. "Introduction to Semiconductor Devices", 2 nd Edition Mc Graw Hill, New York,1981
4. S.M.Sze "Semiconductor Devices - Physics and Technology", John Wiley and sons, 1985.
5. Mohammed Ismail & Terri Fiez "Analog VLSI-Signal & Information Processing" 1st ED,Tata McGraw Hill Publishing company Ltd 2001.

07VL106 TESTING OF VLSI CIRCUITS **3 1 0 100**

UNIT I **9**

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation.

UNIT II **9**

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III **9**

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV **9**

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs

UNIT V **9**

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

L :45 T:15 Total 60

REFERENCES

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design" Jaico Publishing House, 2002.

2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers, 2002.
4. A.L. Crouch, "Design for Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

07VL107 VLSI DESIGN LABORATORY I 0 0 4 100

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Writing Test Benches Using Verilog / VHDL
4. Design and Implementation of ALU using FPGA.
5. Simulation of NMOS and CMOS circuits using SPICE.
6. Design of Static and Dynamic Logic Circuits
7. Modeling of MOSFET using C.
8. Implementation of FFT, Digital Filters.
9. Implementation of DSP algorithms using software package.
10. Implementation of MAC Unit using FPGA.

SEMESTER – II

07VL201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 1 0 100

UNIT I 9 MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES

Depletion region of a pn junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II 9 CIRCUIT CONFIGURATION FOR LINEAR IC

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III 9 OPERATIONAL AMPLIFIERS

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV 9 ANALOG MULTIPLIER AND PLL

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V 9 ANALOG DESIGN WITH MOS TECHNOLOGY

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

L :45 T:15 Total 60

REFERENCES

1. Gray, Meyer, Lewis, Hurst, “Analysis and design of Analog IC’s”, 4th Edition, Wiley International, 2002.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, S.Chand and company ltd, 2000
3. Nandita Dasgupta, Amitava Dasgupta, “Semiconductor Devices,Modelling and Technology”, Prentice Hall of Indiaptvt.ltd,2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, “CMOS Analog Circuit Design”, Second Edition-Oxford University Press-2003

07VL202 COMPUTER AIDED DESIGN OF VLSI CIRCUITS 3 1 0 100

UNIT I 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II	9
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning	
UNIT III	9
Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.	
UNIT IV	9
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.	
UNIT V	9
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.	

L :45
T:15 Total 60

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.
3. Drechsler, R., Evolutionary Algorithms for VLSI CAD, Kluwer Academic Publishers, Boston, 1998.
4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer, Algorithms and Techniques for VLSI Layout Synthesis, Kluwer Academic Publishers, Boston, 1989.

07VL203 VLSI SIGNAL PROCESSING 3 1 0 100

UNIT I	9
INTRODUCTION TO DSP SYSTEMS	
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.	
UNIT II	9
RETIMING, FOLDING AND UNFOLDING	
Retiming - definitions and properties Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques – Register minimization in folded architectures	
UNIT III	9
FAST CONVOLUTION	
Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm – Winograd Algorithm, Iterated Convolution – Cyclic Convolution; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.	
UNIT IV	9
BIT-LEVEL ARITHMETIC ARCHITECTURES	
Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form	

and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

**UNIT V
PROGRAMMING DIGITAL SIGNAL PROCESSORS**

9

Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

L :45 T:15 Total 60

REFERENCES

1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

07VL204 VLSI LAB II

0 0 4 100

- 1.) Implementation of 8 Bit ALU in FPGA / CPLD.
- 2.) Implementation of 4 Bit Sliced processor in FPGA / CPLD.
- 3.) Implementation of Elevator controller using embedded microcontroller.
- 4.) Implementation of Alarm clock controller using embedded microcontroller.
- 5.) Implementation of model train controller using embedded microcontroller.
- 6.) System design using PLL.

**LIST OF ELECTIVES
SEMESTER II**

07VL11 LOW POWER VLSI DESIGN

3 0 0 100

**UNIT I
POWER DISSIPATION IN CMOS**

9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

**UNIT II
POWER OPTIMIZATION**

9

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

UNIT III

9

DESIGN OF LOW POWER CMOS CIRCUITS

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV 9 POWER ESTIMATION

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V 9 SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER

Synthesis for low power –Behavioral level transforms- Software design for low power -

Total: 45

REFERENCES:

1. K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, Designing CMOS Circuits For Low Power, Kluwer,2002
3. J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits,Wiley 1999.
4. A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995.
5. Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6. Abdellatif Bellaouar,Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7. James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

07VL12 CMOS VLSI DESIGN 3 0 0 100

UNIT I 9 MOS TRANSISTOR THEORY

Introduction to I.C Technology. Basic MOS transistors. Threshold Voltage. Body effect. Basic D.C. Equations. Second order effects. MOS models. Small signal A.C characteristics. The complementary CMOS inverter. DC characteristics. Static Load MOS inverters. The differential inverters. Transmission gate.

UNIT II 9 CMOS PROCESSING TECHNOLOGY.

Silicon semiconductor technology. Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology. nwell, pwell process. Silicon on insulator. CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latchup.

UNIT III 9 CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION

Resistance estimation. Capacitance estimation. MOS capacitor characteristics. Device capacitances. Diffusion capacitance. SPICE modeling of MOS capacitance. Routing capacitance. Distributed RC effects. Inductance. Switching characteristics. Rise time. Fall time. Delay time. Empirical delay models. Gate delays. CMOS gate transistor sizing. Power dissipation. Scaling of MOS transistor dimensions.

UNIT IV 9 CMOS CIRCUIT AND LOGIC DESIGN

Cmos Logic gate design. Fan in and fan out. Typical CMOS NAND and NOR delays. Transistor sizing. CMOS logic structures. Complementary logic. BICMOS logic. Pseudo nMOS logic. Dynamic CMOS

logic. Clocked CMOS logic. Pass transistor logic. CMOS domino logic. NP domino logic. Cascade voltage switch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures.

UNIT V
CMOS SUBSYSTEM DESIGN.

9

Data path operations. Addition/subtraction. Parity generators. Comparators. Zero/one detectors. Binary Counters. ALUs. Multiplication. Array, Radix-n, Wallace Tree and Serial Multiplication. Shifters. Memory elements. RWM, Rom, Content Addressable Memory. Control: FSM, PLA Control Implementation.

TOTAL : 45

REFERENCES

1. Neil.H.E. Weste and K.Eshragian, “Principles of CMOS VLSI Design”. 2nd Edition. Addison-Wesley , 2000.
2. Douglas a. Pucknell and K.Eshragian., “Basic VLSI Design” 3rd Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., “CMOS Circuit Design”, 3rd Indian reprint, PHI, 2000.

07VL13 ANALOG VLSI DESIGN

3 0 0 100

UNIT I
BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING:

9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II

9

BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III
SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS

9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators – Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV
DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS

9

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron - Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V
STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND

9

ANALOG AND MIXED ANALOG-DIGITAL LAYOUT

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL : 45

REFERENCES

1. Mohammed Ismail, Terri Fiez, " Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, " Analog VLSI Design - NMOS and CMOS "., Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsvividis, " Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

07VL14 DESIGN OF SEMICONDUCTOR MEMORIES

3 0 0 100

UNIT I

9

RANDOM ACCESS MEMORY TECHNOLOGIES

STATIC RANDOM ACCESS MEMORIES (SRAMs):

SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-BipolarSRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

DYNAMIC RANDOM ACCESS MEMORIES (DRAMs):

DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BiCMOS,DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

UNIT II

9

NONVOLATILE MEMORIES

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-AdvancedFlash Memory Architecture.

UNIT III

9

MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE

RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

UNIT IV

9

SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening andQualification. RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL : 45

REFERENCES

1. S.M.Sze, “VLSI Technology”, Mc.Graw.Hill Second Edition. 1998.
2. Amar mukherjee, “Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000.
3. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India.2000.
4. Wai Kai Chen, 'VLSI Technology' CRC press,2003.

07VL16 PHYSICAL DESIGN OF VLSI CIRCUITS

3 0 0 100

UNIT I

9

INTRODUCTION TO VLSI TECHNOLOGY

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates,field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

UNIT II

9

PLACEMENT USING TOP-DOWN APPROACH

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratiocut- partition with capacity and i/o constraints.

Floor planning: Rectangular dual floor planning- hierarchial approach- simulated annealing- Floor plan sizing-

Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement.

UNIT III

9

ROUTING USING TOP DOWN APPROACH:

Fundamentals: Maze Running- line searching- Steiner trees

Global Routing: Sequential Approaches- hierarchial approaches- multicommodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming

Detailed Routing: Channel Routing- Switch box routing.

Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV

9

PERFORMANCE ISSUES IN CIRCUIT LAYOUT:

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven

Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing

Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization

UNIT V

9

SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

Planar subset problem(PSP)- Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL : 45

REFERENCES

1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995

HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit –protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt processing -Instruction types – Addressing modes – Processor flags – Instruction set -programming the Pentium processor.

UNIT III **9** **HIGH PERFORMANCE RISC ARCHITECTURE :ARM**

The ARM architecture – ARM assembly language program – ARM organization and implementation – The ARM instruction set - The thumb instruction set – ARM CPU cores.

UNIT IV **9** **MOTOROLA 68HC11 MICROCONTROLLERS**

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter – hardware expansion – Assembly language Programming

UNIT V **9** **PIC MICRO CONTROLLER**

CPU architecture – Instruction set - Interrupts – Timers – I/O port expansion –I²C bus for peripheral chip access – A/D converter – UART

Total: 45

REFERENCES :

1. Daniel Tabak , “ Advanced Microprocessors” McGraw Hill.Inc., 1995
 2. James L. Antonakos, “The Pentium Microprocessor “ Pearson Education, 1997.
 3. Steve Furber, “ ARM System –On –Chip architecture “Addison Wesley, 2000.
 4. Gene .H.Miller.” Micro Computer Engineering,” Pearson Education, 2003.
 5. John .B.Peatman, “Design with PIC Microcontroller, Prentice hall, 1997.
 6. James L.Antonakos,” An Introduction to the Intel family of Microprocessors “ Pearson Education 1999.
 7. Barry.B.Breg,” The Intel Microprocessors Architecture , Programming and Interfacing “, PHI, 2002.
 8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001
- Readings :

Web links

www.ocw.nit.edu

www.arm.com

07VL19 NEURAL NETWORKS AND APPLICATIONS **3 0 0 100**

UNIT I **9** **BASIC LEARNING ALGORITHMS:**

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feedforward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering - Beamforming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.

UNIT II **9**
RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES:

RADIAL BASIS FUNCTION NETWORKS:

Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification.

SUPPORT VECTOR MACHINES:

Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem - ϵ -insensitive Loss Function – Support Vector Machines for Nonlinear Regression

UNIT III **9**

ATTRACTOR NEURAL NETWORKS:

Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs - Memory Annihilation of Structured Maps in BAMS – Continuous BAMS – Adaptive BAMS – Applications

UNIT IV **9**

ADAPTIVE RESONANCE THEORY:

Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center –Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory – Applications

UNIT V **9**

SELF ORGANISING MAPS:

Self-organizing Map – Maximal Eigenvector Filtering – Sanger’s Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications

Total: 45

REFERENCES:

1. Satish Kumar, “Neural Networks: A Classroom Approach”, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2004.
2. Simon Haykin, “Neural Networks: A Comprehensive Foundation”, 2ed., Addison Wesley Longman (Singapore) Private Limited, Delhi, 2001.
3. Martin T.Hagan, Howard B. Demuth, and Mark Beale, “Neural Network Design”, Thomson Learning, New Delhi, 2003.
4. James A. Freeman and David M. Skapura, “Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Education (Singapore) Private Limited, Delhi, 2003.
5. S. Rajasekaran, G.A. Vijayalakshmi Pai, Neural Networks, Fuzzy Logic and Genetic Algorithms, Synthesis and Applications, Prentice –Hall of India, New Delhi,2003.

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II

9

RELIABILITY PREDICTION, MODELLING AND DESIGN

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III

9

ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity , fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV

9

RELIABILITY TESTING AND ANALYSIS

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V

9

MANUFACTURE AND RELIABILITY MAQNAGEMENT

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL : 45

REFERENCES

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

07VL22 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN 3 0 0 100

UNIT I

9

EMI ENVIRONMENT

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT II

9

EMI COUPLING PRINCIPLES

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT III **9**
EMI/EMC STANDARDS AND MEASUREMENTS

Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

UNIT IV **9**
EMI CONTROL TECHNIQUES

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT V **9**
EMC DESIGN OF PCBs

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

TOTAL : 45

REFERENCES

1. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, NewYork. 1988.
2. C.R.Paul, "Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992
3. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1996.
4. Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed, 1986.

07VL23 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING 3 0 0 100

UNIT I **9**
FUNDAMENTALS OF PROGRAMMABLE DSPs

Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II **9**
TMS320C3X PROCESSOR

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT III **9**
ADSP PROCESSORS

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT IV **9**
ADVANCED PROCESSORS I

Architecture of TMS320C54X: Pipe line operation, Addressing modes and assembly language instructions
Introduction to Code Composer studio

**UNIT V
ADVANCED PROCESSORS II**

9

Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL : 45

REFERENCES

1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
2. User guides Texas Instrumentation, Analog Devices, Motorola.

07VL24

DATA CONVERTERS

3 0 100

UNIT I

Data Conversion Fundamental, Data Converter Performances

9

Sampling of Analog Signals-Quantization Error and Quantization Noise-Nyquist Rate and Oversampling Conversion-Resolution and SNR-Reconstruction-Static Performances-Dynamic Performances-Distortion and SFDR

UNIT II

Sample and Hold Circuits, Low Speed Nyquist-rate A/D Converters

9

CMOS Track and Sample and Hold-Diode Bridge T&H-Switched Emitter T&H-Accuracy and Speed-Integrating Converter-Successive Approximation Converters-Algorithmic A/D Converters

UNIT III

High Speed Nyquist-rate A/D Converters, Oversampling A/D Converters

9

Flash Converters-Two-Step Converters-Folding Converters-Interpolating Technique-Interleaved Converters-Pipeline Converters-Noise Shaping-First-Order Sigma-Delta - Second-Order Sigma-Delta - High-Order Sigma-Delta-Multibit Oversampling Converters-Practical Limit-Design Considerations

UNIT IV

Digital Correction and Calibration, Nyquist-rate D/A

9

Digital-Correction-Linearization of Transfer Characteristics-Basic considerations-Switched-Capacitor MDAC-Resistive-based Architectures-Current Steering D/A Converters

UNIT V Over sampling D/A Converters, Data Converter Applications, Hardware Design Techniques

9

Single-Bit solutions-Multi-bit Solutions- Precision Measurement and Sensor- Conditioning - Multichannel Data Acquisition Systems- Digital Potentiometers- Digital Audio-Digital Video and Display Electronics-Software Radio and IF Sampling-Direct Digital Synthesis (DDS)-Precision Analog Microcontrollers-Passive Components- PC Board Design Issues-Analog Power Supply Systems- Over voltage Protection- Thermal Management- EMI/RFI Considerations- Low Voltage Logic Interfacing-Bread boarding and Prototyping.

References

1. D.A. Johns and K. Martin, “Analog Integrated Circuits and Systems, McGraw-Hill, NY 1994
2. Rudy J, Van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” BS Publications” 2005.
3. B. Razavi, Principles of Data Conversion System Design, The IEEE Press, New York, 1995.
4. Analog-Digital Conversion, Walt Kester, Editor, analog devices, 2004

UNIT I**INTRODUCTION, RANDOM SIGNALS AND NOISES, INTRODUCTION TO LOW NOISE AMPLIFIERS 9**

Introduction to RF IC design, Gain, decibels, impedance levels, non linearities and harmonic distortions, intermodulation, dynamic range, introduction to random process and noises, review of thermal noise, noise models and circuit noise calculations, low noise RF amplifiers structures, relationship between power consumption, gain, linearity and noise figures.

UNIT II Non linear RF circuits and systems, RF mixers 9

Non linear elements, their characteristics and approximation methods, harmonics analysis of current in non linear elements, non linear resonant amplifiers and frequency multipliers, Up and down conversion mixers, single and double balanced mixers

UNIT III RF oscillators, Multiples access techniques 9

Oscillators, types of oscillators, feedback oscillator topologies, resonant oscillators, crystal oscillators, small signal analysis of an oscillators, short introduction to voltage controlled oscillators, frequency division multiple access(FDMA), time division multiple access(TDMA), Code division multiple access(CDMA).

UNIT IV Modulators and demodulators techniques, RF transceivers architectures 9

Modulators and demodulators, their structures and electrical schemes, transceivers and architectures, Transceivers functions and their characteristics, direct conversions and super heterodyne receivers.

UNIT V Phase Locked Loops (PLL) 9

Phase locked loops and frequency synthesis, Basic building block of the PLL, PLL synthesizers for radio applications.

References

1. D. M. Pozar, Microwave engineering, 2nd edition, N.Y., John Wiley and Sons, 1998
2. B.P.Lathi, Modern digital and analog communication systems, 3rd edition, N.Y., Oxford University press, 1998
3. B.Sklar, Digital communications-fundamentals and applications, 2nd edition, Prentice Hall PTR, New Jersey, 2001.

07VL26 Analysis and Design of Digital Integrated Circuits**3 0 0 100****UNIT I****DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES-MOS AND BIPOLAR, FABRICATION, LAYOUT AND SIMULATION 9**

Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology-Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology

UNIT II**MOS INVERTER CIRCUITS, STATIC MOS GATE CIRCUITS 9**

Voltage transfer characteristics-noise margin definitions-resistive load inverter design-NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate

circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip-flops and latches – power dissipation in CMOS gates-power and delay trade-offs.

UNIT III

HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN

9

Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping.

UNIT IV

SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORY DESIGN, INTERCONNECT DESIGN

9

Introduction-MOS decoders – static RAM cell design-SRAM column I/O circuitry – memory architecture-content addressable memories-FPGA-dynamic Read-Write memories-Read Only memories-EPROMs and E²PROMs-flash memory-FRAMs-interconnect RC delays-buffer insertion for very long wires-interconnect coupling capacitance-interconnect inductance-antenna effects.

UNIT V

POWER GRID AND CLOCK DESIGN, LOW POWER CMOS LOGIC CIRCUITS, CHIP INPUT AND OUTPUT CIRCUITS, DESIGN FOR TESTABILITY

9

Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise – on-chip clock generation and distribution – latch-ups and its prevention – fault types and models – controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring I_{DDQ} test.

REFERENCES:

1. David A Hodges, Horace G Jackson, Resve A Saleh, “Analysis and design of Digital Integrated Circuits – in deep submicron technology”, Tata McGraw Hill, Edition 2005.
2. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits-analysis and design”, Tata McGraw Hill, Third edition-2003

07VL27 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

3 0 0 100

UNIT I

PRINCIPLES OF PARALLEL PROCESSING

9

Multiprocessors and Multicomputers – Multivector and SIMD Computers- PRAM and VLSI Models-Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- parallel processing applications- speed up performance law.

UNIT II

PROCESSOR AND MEMORY ORGANIZATION

9

Advanced processor technology – Superscalar and vector processors- Memory hierarchy technology-Virtual memory technology- Cache memory organization- Shared memory organization.

UNIT III

PIPELINE AND PARALLEL ARCHITECTURE

9

Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design-Superscalar and super pipeline design- Multiprocessor system interconnects- Message passing

mechanisms.

UNIT IV
VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE

9

Vector Processing principle- Multivector Multiprocessors- Compound Vector processing- Principles of multithreading-fine grain multicomputers- scalable and multithread architectures – Dataflow and hybrid architectures.

UNIT V
SOFTWARE AND PARALLEL PROCESSING

9

Parallel programming models- parallel languages and compilers- parallel programming environments- synchronization and multiprocessing modes- message passing program development- mapping programs onto multicomputers- multiprocessor UNIX design goals- MACH/OS kernel architecture- OSF/1 architecture and applications.

TOTAL : 45

REFERENCES

1. Kai Hwang, Advanced Computer Architecture, TMH 2001.
2. William Stallings, Computer Organization and Architecture, McMillan Publishing Company, 1990.
3. M.J. Quinn, Designing efficient Algorithms for parallel computer, McGraw Hill International, 1994.

07VL28 EMBEDDED SYSTEMS

3 0 0 100

UNIT I

9

EMBEDDED ARCHITECTURE

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded System Design, Embedded System Design Process - Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration.

UNIT II

9

EMBEDDED PROCESSOR AND COMPUTING PLATFORM

ARM processor- processor and memory organization, data operations, flow of control, SHARC processor- memory organization, data operations, flow of control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory Devices, Input / Output Devices. Design Example: Alarm Clock.

UNIT III

9

NETWORKS

Distributed Embedded Architecture - Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet. Design Example: Elevator Controller.

UNIT IV

9

REAL-TIME CHARACTERISTICS

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, Off-line Versus On-line scheduling.

UNIT V

SYSTEM DESIGN TECHNIQUES

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX-Ink jet printer- Personal Digital Assistants, Set-top Boxes.

TOTAL : 45**REFERENCES**

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufman Publishers, 2001.
2. Jane.W.S. Liu Real-Time systems, Pearson Education Asia, 2000
3. C. M. Krishna and K. G. Shin , Real-Time Systems, ,McGraw-Hill, 1997
4. Frank Vahid and Tony Givargi, Embedded System Design: A Unified Hardware/Software Introduction, s, John Wiley & Sons, 2000.

07VL29**RF MEMS****3 0 0 100****UNIT I: SWITCHING**

RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

UNIT II: COMPONENTS - I

MEMS inductors and capacitors: Micromachined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

UNIT III: COMPONENTS - II

MEMS phase shifters: Types. Limitations, Switched delay lines, Micromachined transmission lines, coplanar lines, Micromachined directional coupler and mixer.

UNIT IV: FILTERS

Micromachined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures.

UNIT V: ANTENNAS

Micromachined antennas: Microstrip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

TEXT BOOK:

1. *V.K.Varadan etal, RFMEMS and their Applications, Wiley, 2003.*
2. H.J.DELOS SANTOS : RF MEMS circuit Design for Wireless Communications, Artech House, 2002.
3. G.M.REBEIZ : RF MEMS Theory, Design and Technology, John Wiley, 2003