

**ANNA UNIVERSITY - COIMBATORE – 13**

**CURRICULUM - 2007**

**FACULTY OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**Branch : M.E. (EMBEDDED SYSTEM TECHNOLOGIES)**

**SEMESTER – I (FULL- TIME)**

Subject Code	Subject Name	Hours / Week			
		L	T	P	M
<b>THEORY</b>					
ECM 101	Applied Mathematics	3	1	0	100
ECE 104	Advanced Digital System Design	3	1	0	100
EES 101	Advanced Embedded Systems I	3	0	0	100
EES 102	Advanced Digital Signal Processing	3	0	0	100
EES 103	Microcontroller System Design & Applications	3	0	0	100
EES 104	Software Technology for Embedded Systems	3	0	0	100
<b>PRACTICALS</b>					
EES 105	Embedded System Lab I	0	0	3	100
	<b>TOTAL</b>	<b>18</b>	<b>2</b>	<b>3</b>	<b>700</b>

**SEMESTER – II (FULL- TIME)**

Subject Code	Subject Name	Hours / Week			
		L	T	P	M
<b>THEORY</b>					
EES 201	Real Time Embedded Operating System	3	1	0	100
EES 202	Embedded Networking	3	1	0	100
EES 203	Embedded Control Systems	3	0	0	100
	Elective I	3	0	0	100
	Elective II	3	0	0	100
	Elective III	3	0	0	100
<b>PRACTICALS</b>					
EES 204	Embedded System Lab II	0	0	3	100
	<b>TOTAL</b>	<b>18</b>	<b>2</b>	<b>3</b>	<b>700</b>

**SEMESTER – III (FULL- TIME)**

Subject Code	Subject Name	Hours / Week			
		L	T	P	M
<b>THEORY</b>					
	Elective IV	3	0	0	100
	Elective V	3	0	0	100
	Elective VI	3	0	0	100
<b>PRACTICALS</b>					
EES 301	Project Work - Phase I	0	0	12	200
	<b>TOTAL</b>	<b>9</b>	<b>0</b>	<b>12</b>	<b>500</b>

**SEMESTER – IV (FULL- TIME)**

Subject Code	Subject Name	Hours / Week			
		L	T	P	M
<b>PRACTICALS</b>					
EES 401	Project Work - Phase II	0	0	24	400
	<b>TOTAL</b>	<b>0</b>	<b>0</b>	<b>24</b>	<b>400</b>

**LIST OF ELECTIVES**For **SEMESTER II (ELECTIVE – I, ELECTIVE – II AND ELECTIVE – III)**

Subject Code	Subject Name	Hours / Week			
		L	T	P	M
ECE 103	Data Communication & Networks	3	0	0	100
ECE E02	Digital Image Processing	3	0	0	100
ECE E14	ASIC Design	3	0	0	100
EES E01	Advanced Embedded Systems-II	3	0	0	100
EES E02	Computer Architecture	3	0	0	100
EES E03	Cryptography and Network Security	3	0	0	100
EES E04	Multimedia Systems	3	0	0	100
EES E05	Operating Systems	3	0	0	100
EES E06	VHDL	3	0	0	100
EES E07	Wireless & Mobile Communication	3	0	0	100

## SEMESTER - I

### ECM 101 APPLIED MATHEMATICS

**L T P M**  
**3 1 0 100**

(Common to Communication Systems, Computer & Communication, Embedded System Technologies , Medical Electronics, Network Engineering and VLSI Design)

#### **UNIT - I LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEMS (12)**

System of equations- Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method- Jacobi, Gauss-Seidal iteration method- Eigen values of a matrix by Jacobi and Power method.

#### **UNIT - II WAVE EQUATION (12)**

Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

#### **UNIT - III SPECIAL FUNCTIONS (12)**

Bessel's equation - Bessel Functions- Legendre's equation - Legendre polynomials - Rodrigue's formula - Recurrence relations- generating functions and orthogonal property for Bessel functions - Legendre polynomials.

#### **UNIT - IV RANDOM VARIABLES (12)**

One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient - Functions of Two dimensional random variable

#### **UNIT - V QUEUEING THEORY (12)**

Single and Multiple server Markovian queueing models - Steady state system size probabilities – Little's formula - Priority queues - M/G/1 queueing system – P.K. formula.

**Lecture 45 Tutorial 15 Total 60**

#### **Reference Books**

- 1 Sankara Rao.K. "Introduction to Partial Differential Equation ", PHI, 1995.
- 2 Taha. H.A., "Operations Research- An Introduction " 6<sup>th</sup> Edition, PHI, 1997.
- 3 Jain M.K. Iyengar, S.R.K. & Jain R.K., "International Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publishers 2003.
- 4 Kanpur J.N. & Saxena. H.C. "Mathematical Statistics", S.Chand & Co.,New Delhi, 2003.
- 5 Greweal B.S. "Higher Engineering Mathematics", Khanna Publishers, 2005.

## **ECE 104 ADVANCED DIGITAL SYSTEM DESIGN**

**L T P M**  
**3 1 0 100**

(Common to Embedded System Technologies and VLSI Design)

### **UNIT - I SEQUENTIAL CIRCUIT DESIGN (12)**

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

### **UNIT - II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (12)**

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

### **UNIT - III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (12)**

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

### **UNIT - IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (12)**

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

### **UNIT - V SYSTEM DESIGN USING VHDL (12)**

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modelling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

### **Reference Books**

**Lecture 45 Tutorial 15 Total 60**

- 1 Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
- 2 John M Yarbrough "Digital Logic appns. and Design" Thomson Learning, 2001
- 3 Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001
- 4 Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
- 5 Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
- 6 Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Deisgn" Tata McGraw Hill, 2002.
- 7 Navabi.Z. "VHDL Analysis and Modeling of Digital Systems. McGraw International, 1998.
- 8 Parag K Lala, "Digital System design using PLD" BS Publications, 2003
- 9 Parag K Lala, " Digital Circuit Testing and Testability" Academic Press, 1997.
- 10 Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India (P) Ltd, 2002
- 11 Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004
- 12 Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996.
- 13 Nelson V.P., Nagale H.T., Carroll B.D., and Irwin J.D., "Digital Logic Circuit Analysis and Design", Prentice Hall International Inc.1995.
- 14 Dueck R.K., "Digital Design with CPLD applications and VHDL" Thomson Delmer Learning, 2001.

**UNIT - I PRINCIPLES OF EMBEDDED SYSTEM (9)**

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture - Categories of Embedded Systems - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques. **Wired Communication Protocols:** UART - Inter Integrated Circuit (I<sup>2</sup>C) - Serial Peripheral Interface (SPI) - Controller Area Network (CAN). **Wireless communication Protocols:** Zigbee Protocols – Blue tooth Protocols - IrDA.

**UNIT - II ARM PROCESSOR FUNDAMENTALS (9)**

ARM core Introduction – Registers – Current Program Status Register – Pipeline – Exception – Interrupts – Vector Table – Core Extension – Architecture Revisions – ARM Processor Families – ARM Instruction Set – Thumb Instruction set - Thumb Register Usage – ARM – Thumb Interworking – Stack Instruction - Software Interrupt Instruction.

**UNIT - III CACHES AND MMU (9)**

The Memory Hierarchy and Cache Memory – Cache Architecture - Cache Policy – Co Processor and Caches – Flushing and Cleaning Cache Memory – Cache Lockdown – Caches and Software Performance. **MMU:** Moving from an MPU to an MMU – Virtual Memory – Details of ARM MMU – The Caches and Write Buffer – Co Processor and MMU configuration.

**UNIT - IV OPTIMIZED PRIMITIVES (9)**

Double Precision Integer Multiplication – Integer Normalization and count Leading Zeros – Division – Square Roots – Transcendental Functions : Log,,exp,sin,cos – Endian Reversal and Bit Operations – Saturated and Rounded Arithmetic - Random Number Generation

**UNIT - V WRITING AND OPTIMIZING ARM ASSEMBLY CODE (9)**

Writing Assembly Code – Profiling and Cycle Counting – Instruction Scheduling – Register Allocation – Conditional Execution – Looping Constructs – Bit Manipulation – Efficient Switches – Handling Unaligned Data.

**Total 45****Reference Books**

- 1 Andrew N.Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide”, Morgan Kaufmann Series in Computer Architecture and Design, 2004.
- 2 Tammy Noergaard, “Embedded Systems Architecture”, Newnes, 2005.
- 3 David Seal, “ARM Architecture Reference Manual”, 2005.
- 4 Steve Furbe, “ARM System-on-Chip Architecture”, Addison-Wesley Professional, 2nd Edition, 2000.

[Review of discrete-time signals and systems- DFT and FFT, Z-Transform, Digital Filters is recommended]

**UNIT - I DISCRETE RANDOM SIGNAL PROCESSING (9)**

Discrete Random Processing – Expectations – Variance – Co-Variance – Scalar Product – Energy of Discrete Signals – Parseval’s Theorem – Wiener Khintchine Relation – Power Spectral Density – Periodogram. Autocorrelation – Sum Decomposition Theorem – Spectral Factorization Theorem – Discrete Random Signal Processing by Linear Systems – Simulation of White Noise – Low Pass Filtering of White Noise.

**UNIT - II LINEAR ESTIMATION AND PREDICTION (9)**

Maximum likelihood criterion – Efficiency of estimator – Least Mean Squared Error Criterion – Wiener Filter – Discrete Wiener Hoff Equations – Recursive estimators – Kalman filter – Linear prediction – Prediction error – Whitenign fliter – Inverse filter – Levinson recursion – Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

**UNIT - III ADAPTIVE FILTERS (9)**

FIR adaptive filters – Newton’s steepest descent method – Adaptive filter based on steepest descent method – Widrow Hoff LMS adaptive algorithm – Adaptive channel equalization – Adaptive echo cancellor – Adaptive noise cancellation – RLS Adaptive filters – Exponentially weighted RLS – Sliding window RLS – Simplified HR LMS adaptive filter.

**UNIT - IV MULTIRATE DIGITAL SIGNAL PROCESSING (9)**

Mathematical description of change of sampling rate – Interpolation and Decimation – Continuous time model – Direct digital domain approach – Decimation by an integer factor – Interpolation by an integer factor – Single and multistage realization – Poly phase realization – Application to sub band coding – Wavelet transform and filter bank implementation of wavelet expansion of signals.

**UNIT - V DIGITAL SIGNAL PROCESSORS (9)**

Fundamentals of Fixed – Point DSP Architecture – Fixed Point Representation of Numbers – Arithmetic Computation – Memory Accessing – Pipelining of Instructions – Features of Example Processors – TMS320C25 – DSP16A and DSP 56001 – Floating Point DSPs – Floating-Point Representation of Numbers – TMS320C30 – Comparison of DSPs – Development Tools for DSP Programming – TMS320C30 Evaluation Module.

**Reference Books****Total 45**

- 1 Monson H. Hayes, ‘Statistical Digital Signal Processing and Modeling’, John Wiley and Sons Inc., New York, 1996.
- 2 Sopocles J. Orfanidis, ‘Optimum Signal Processing’, McGraw Hill, 1990.
- 3 John G. Proakis, Dimitirs G. Monolakis, ‘Digital Signal Processing’, Pearson Education, 1995.
- 4 Sanjit K. Mitra, ‘Digital Signal Processing – A Computer based approach’, Tata McGraw Hill – 1998.
- 5 Rabiner and Gold, ‘Theory and Applications of Digital Signal Processing, A Comprehensive, Industrial – Strength DSP reference book’
- 6 TMS320C5X User’s Guide, Texas Instruments, 1995.

## EES 103 MICROCONTROLLER SYSTEM DESIGN AND APPLICATIONS

L T P M  
3 0 0 100

### **UNIT - I 8051 ARCHITECTURE (9)**

Basic organization – 8051 CPU structure – Register file – Interrupts – Timers – Port circuits – Instruction set – Timing diagram – Addressing modes – Simple Program and Applications.

### **UNIT - II PERIPHERALS AND INTERFACING (9)**

Typical Bus structure – Bus – memory organization – Timing characteristics – Extended Model and Memory Interfacing – Polling – Interfacing Basic I/O devices – Analog and Digital interfacing – PWM mode operation – Serial port application.

### **UNIT - III 8096 ARCHITECTURE (9)**

CPU operation – Interrupt structure – Timers – High Speed Input / Output Ports – I/O control and Status registers – Instruction Set – Addressing Modes – Simple Programming – Queues – Tables and Strings – Stack Memories – Key Switch – Parsing.

### **UNIT - IV PERIPHERALS AND INTERFACING (9)**

Analog Interface – Serial Ports – Watch dog timers – Real Time Clock – Multitasking – Bus Control – Memory Timing – External ROM and RAM expansion – PWM control – A/D interfacing.

### **UNIT - V CASE STUDY FOR 8051 AND 8096 (9)**

Real Time clock – DC Motor Speed Control – Generation of Gating Signals for Converters and Inverters – Frequency Measurement – Temperature Control

**Total 45**

### **Reference Books**

- 1 John B.Peatman, "Design with Micro controllers", McGraw Hill international Limited, Singapore, 1989.
- 2 Michael Slater, "Microprocessor based design A comprehensive guide to effective Hardware design" Prentice Hall, New Jersey, 1989.
- 3 Ayala, Kenneth, "The 8051 Microcontroller" Upper Saddle River, New Jersey Prentice Hall, 2000.
- 4 Intel Manual on 16 bit embedded controllers, Santa Clara, 1991.
- 5 Muhammad Ali Mazidi, Janice Gillispie mazidi. "The 8051 Microcontroller and Embedded systems", Person Education, 2004.

**UNIT - I      BASIC CONCEPTS IN OBJECT-ORIENTED METHODOLOGY      (9)**

Benefits of object-oriented methodology. Class & Objects - Definitions - How to determine the object and classes, where to look, what to look for, what to consider and challenge, examples. Identifying structures: Definitions - generalization - specialization, whole-part structures, examples. Definitions - examples. Defining attributes - Definitions - How to determine the attributes, Instance connections, examples. Defining services, message connections, specifying services, final class and object specification examples.

**UNIT - II      OBJECT ORIENTED ANALYSIS      (9)**

Connecting the Object Model with the Use Case Model - Key strategies for Object – Identification – Underline the Noun strategy. Identify the Casual Objects – Identify Services (Passive Contributors) – Identify Real-World Items – Identify Physical Devices – Identify Key Concepts – Identify Transactions – Identify persistent information – Identify visual elements – Identify control elements – Apply scenarios

**UNIT - III      OBJECT ORIENTED SYSTEMS DEVELOPMENT      (9)**

Introduction to object oriented systems development – Procedure oriented paradigms – Procedure oriented development tools – Object Oriented paradigm – Object Oriented notations and graphs – Steps in Object Oriented Analysis – Steps in Object Oriented analysis – Steps in Object Oriented design – Prototyping paradigm - Approach to Object Oriented Design – The programming problem – The CRC modeling team – Constructing the CRC cards – Use Cases – Class relationships – Class Diagrams

**UNIT - IV      UNIFIED MODELING LANGUAGE      (9)**

Object state behaviour – UML state charts – Role of scenarios in the definition of behaviour – Timing diagrams – Sequence diagrams – Event hierarchies – Types and strategies of operations – Architectural design in UML concurrency design – Representing tasks – System task diagram – Concurrent state diagrams – Threads – Mechanistic design – Simple patterns.

**UNIT - V      CASE STUDIES      (9)**

Multi threaded applications – Assembling embedded applications – Polled waiting loop and interrupt driven I/O – Preemptive kernels and shared resources – System timer – Scheduling – Client server computing

**Total      45**

**Reference Books**

- 1 Peter Coad and Edward Yourdon, “Object Oriented Analysis”, PH, 2<sup>nd</sup> Edn.,1991
- 2 Peter Coad and Edward Yourdon, “Object Oriented Design”, PH, 1991.
- 3 Bruce Powel Douglas, “Real-Time UML: Developing Efficient Objects for Embedded Systems” 2<sup>nd</sup> Edition, Addison – Wesley, 1999.
- 4 Hassan Gomma, “Designing concurrent, distributed, and Real-Time applications with UML”
- 5 Robert Lafore, “Object Oriented Programming in C++”, Galgotia Publications Pvt. Ltd., 3<sup>rd</sup> Edition, 2001

## PRACTICALS

### EES 105 EMBEDDED SYSTEMS LAB I

L	T	P	M
0	0	3	100

#### LIST OF EXPERIMENTS

- 1 Micro controller 8051/8031/8096 & Flash controller programming
  - (a) Simple application programs with kit and through assembler
  - (b) Data flash with erase, verify, fusing through ATMEL and INTEL tools.
  
- 2 Testing RTOS Environment and System Programming.
  - (a) Keil Tools
  - (b) RTOS System Solutions with Tornado tools.
  
- 3 Complex Programmable Logic Devices and Device Programming with VHDL fitter and Cool runner
  - (a) Warp tools-Cypress-Active HDL Simulator & Galaxy-VHDL, FSM models
  - (b) Mixed signal handling.
  
- 4 Third party design tools
  - (a) Mentor Graphics
  - (b) Cadence.
  - (c) Model Sim

**Total 45**

## SEMESTER - II

<b>EES 201 REAL TIME EMBEDDED OPERATING SYSTEMS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>M</b>
	<b>3</b>	<b>1</b>	<b>0</b>	<b>100</b>

### **UNIT - I INTRODUCTION TO EMBEDDED SYSTEM** (12)

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture (**CISC and RISC**) - Categories of Embedded Systems - embedded processor selection & tradeoffs - Embedded design life cycle - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques – ARM 7

### **UNIT - II OPERATING SYSTEM OVERVIEW** (12)

Introduction – Advantage and Disadvantage of Using RTOS – Multitasking – Tasks - Real Time Kernels – Scheduler - Non-preemptive Kernels - Preemptive Kernels – Reentrancy- Reentrant Functions – Round Robin Scheduling - Task Priorities - Static Priorities – Mutual Exclusion – Deadlock – Intertask Communication – Message Mailboxes – Message Queues - Interrupts - Task Management – Memory Management - Time Management – Clock Ticks.

### **UNIT - III** (12)

Introduction -  $\mu$ C/OS-II Features - Goals of  $\mu$ C/OS-II - Hardware and Software Architecture – **Kernel Structures:** Tasks – Task States – Task Scheduling – Idle Task – Statistics Task – Interrupts Under  $\mu$ C/OS-II – Clock Tick -  $\mu$ C/OS-II Initialisation. **Task Management:** Creating Tasks – Task Stacks – Stack Checking – Task's Priority – Suspending Task – Resuming Task. **Time Management:** Delaying a Task – Resuming a Delayed Task – System Time. Event Control Blocks- Placing a Task in the ECB Wait List – Removing a Task from an ECB wait List .

### **UNIT - IV** (12)

**Semaphore Management:** Semaphore Management Overview – Signaling a Semaphore. **Message Mailbox Management:** Creating a Mailbox – Deleting Mailbox – Waiting for a Message box – Sending Message to a Mailbox- Status of Mailbox . **Message Queue Management:** Creating Message Queue – Deleting a Message Queue – Waiting for a Message at a Queue – Sending Message to a Queue – Flushing a Queue.

### **UNIT - V** (12)

**Memory Management:** Memory Control Blocks – Creating Partition- Obtaining a Memory Block – Returning a Memory Block . Getting Started with  $\mu$ C/OS-II – Installing  $\mu$ C/OS-II – **Porting  $\mu$ C/OS-II:** Development Tools – Directories and Files – Testing a Port - IAR Workbench with  $\mu$ C/OS-II -  $\mu$ C/OS-II Porting on a 8051 CPU – Implementation of Multitasking - Implementation of Scheduling and Rescheduling – Analyze the Multichannel ADC with help of  $\mu$ C/OS-II.

**Reference Books** **Lecture 45 Tutorial 15 Total 60**

- 1 Jean J. Labrosse, MicroC/OS – II The Real Time Kernel, CMP Books, 2<sup>nd</sup> Edition 1998.
- 2 David Seal, ARM Architecture Reference Manual, 2005.
- 3 Steve Furbe, ARM System-on-Chip Architecture, Addison-Wesley Professional, 2 edition 2000.

**UNIT - I** (12)

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

**UNIT - II** (12)

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

**UNIT - III** (12)

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.

**UNIT - IV** (12)

Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.

**UNIT - V** (12)

.Implementation issues – Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

**Lecture 45 Tutorial 15 Total 60****Reference Book**

- 1 Glaf P.Feiffer, Andrew Ayre and Christian Keyold “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.

**UNIT - I INTRODUCTION (6)**

Controlling the hardware with software – Data lines – Address lines - Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

**UNIT - II INPUT-OUTPUT DEVICES (8)**

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules – LCD module display – Configuration – Time-of-day clock – Timer manager - Interrupts - Interrupt service routines – IRQ - ISR - Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

**UNIT - III D/A AND A/D CONVERSION (12)**

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

**UNIT - IV ASYNCHRONOUS SERIAL COMMUNICATION (9)**

Asynchronous serial communication – RS-232 – RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module - Buffered serial I/O.

**UNIT - V CASE STUDIES: EMBEDDED C PROGRAMMING (10)**

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

**Total 45****Reference Books**

- 1 Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C" The publisher, Paul Temme, 1999.
- 2 Ball S.R., 'Embedded microprocessor Systems – Real World Design', Prentice Hall, 1996.
- 3 Herma K, "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997.
- 4 Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet", PHI, 2002.

## PRACTICALS

**EES 204**

**EMBEDDED SYSTEMS LAB II**

<b>L</b>	<b>T</b>	<b>P</b>	<b>M</b>
<b>0</b>	<b>0</b>	<b>3</b>	<b>100</b>

### LIST OF EXPERIMENTS

- 1 VLSI designing with various Tools and Design methodologies
  - (a) AT40K FPGA series-synthesis-design-simulation of application programs.
  - (b) Xilinx EDA design tools-device programming –PROM programming.
  - (c) ALTERA and Mentor graphics-IC design tools.
  
- 2 Embedded DSP based System Designing.
  - (a) Analog DSP tool kit.
  - (b) Code compressor studio for embedded DSP using Texas tool kit.
  
- 3 IPCORE usage in VOIP Through SoC2 tools
  - (a) Cypress PsoC designing Tools
  - (b) SoPC designing Tools
  
- 4
  - (a) Intel 8086 Assembly Language Programming using 8086 Assembler
  - (b) MPLAB for assembly programming & PIC

**Total 45**

## LIST OF ELECTIVES

For SEMESTER – II (ELECTIVE – I, ELECTIVE – II and ELECTIVE – III)

<b>ECE 103 DATA COMMUNICATION AND NETWORKS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>M</b>
	<b>3</b>	<b>0</b>	<b>0</b>	<b>100</b>

### **UNIT - I INTRODUCTION (9)**

Components of network – Topologies – WAN / LAN – OSI – ISO layered Architecture Modulation and demodulation – Bit error rates – Line coding – Error correcting codes.

### **UNIT - II DATA LINK LAYER (9)**

Design issues – CRC technique and sliding window techniques – Performance analysis of sliding window techniques – Framing formats – Case Study – HDLC protocols – Medium access control – CSMA / CD – Token ring and token bus – FDDI – Wireless LAN – Performance analysis of MAC protocols – Bridges.

### **UNIT - III NETWORK LAYER (9)**

Circuit switching – packet switching – Design issues – IP addressing and IP diagram – Routers and gateways – Routing – Sub netting – CIDR – ICMP – ARP – RARP – Ipv6 – QoS.

### **UNIT - IV TRANSPORT LAYER (9)**

TCP and UDP – Error handling and flow control – Congestion control – TCP Retransmission – Timeout – Socket Abstraction.

### **UNIT - V APPLICATION SERVICES (9)**

Simple Mail Transfer Protocol (SMTP) – File Transfer Protocols (FTP), telnet, the World Wide Web (WWW), Hypertext Transfer Protocol (HTTP), Domain name service (DNS), Security, Multimedia applications.

**Total 45**

### **Reference Books**

- 1 William Stallings, "Data and Computer Communications", Seventh Edition, Prentice Hall, 2003.
- 2 Larry Peterson, Bruce S Davie "Computer Networks: A Systems Approach", Morgan Kaufmann Publishers, 2<sup>nd</sup> Edition, 1999
- 3 James F Kurose, "Computer Networking: A Top – Down Approach Featuring the Internet", Addison Wesley, 2<sup>nd</sup> Edition 2002.
- 4 W.Richard Stevens and Gary R Wright, "TCP / IP Illustrated", Addison Wesley, Volume 1 & 2, 2001.
- 5 Douglas E Corner, "Internetworking with TCP / IP", Volume 1 & 2, 2000.

**UNIT - I DIGITAL IMAGE FUNDAMENTALS (9)**

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals -RGB,HSI models, Image acquisition and sampling, Quantization, Image file formats, Two-dimensional convolution, correlation, and frequency responses.

**UNIT - II IMAGE TRANSFORMS (9)**

1D DFT, 2D transforms – DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Radon, and Wavelet Transform.

**UNIT - III IMAGE ENHANCEMENT AND RESTORATION (9)**

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic filters, Homomorphic filtering, Color image enhancement. Image Restoration – degradation model, Unconstrained and Constrained restoration, Inverse filtering, Wiener filtering, Geometric transformations– spatial transformations, Gray-Level interpolation,

**UNIT - IV IMAGE SEGMENTATION AND RECOGNITION (9)**

Edge detection. Image segmentation by region growing, region splitting and merging, edge linking, Morphological operators: dilation, erosion, opening, and closing. Image Recognition–Patterns and pattern classes, matching by minimum distance classifier, Statistical Classifier. Matching by correlation, Neural network application for image recognition.

**UNIT - V IMAGE COMPRESSION (9)**

Need for image compression, Huffman, Run Length Encoding, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT and Wavelet. Image compression standards.

**Total 45****Reference Books**

- 1 Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
- 2 Anil K.Jain,'Fundamentals of Digital Image Processing',Prentice Hall of India,02.
- 3 David Salomon : Data Compression – The Complete Reference, Springer Verlag New York Inc., 2<sup>nd</sup> Edition, 2001
- 4 Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
- 5 William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
- 6 Milman Sonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
- 7 Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.
- 8 Lim, J.S., 'Two Dimensional Signal and Image Processing', Prentice-Hall, New Jersey, 1990.

**UNIT - I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN (9)**

Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

**UNIT - II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS (9)**

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

**UNIT - III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY. (9)**

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

**UNIT - IV LOGIC SYNTHESIS, SIMULATION AND TESTING (9)**

Verilog and logic synthesis – VHDL and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

**UNIT - V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING (9)**

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC.

**Total 45**

**Reference Books**

- 1 M.J.S. SMITH, "Application – Specific Integrated Circuits" – Addison – Wesley Longman Inc., 1997.
- 2 Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
- 3 S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, "Field Programmable Gate Arrays" – Kluver Academic Publishers, 1992.
- 4 Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
- 5 S.Y. Kung, H.J.Whilo House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
- 6 Jose E.France, Yannis Tsvividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

**UNIT - I INTRODUCTION AND REVIEW OF EMBEDDED HARDWARE (9)**

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Round-Robin – Round Robin with interrupt function – Rescheduling architecture – algorithm.

**UNIT - II REAL TIME OPERATING SYSTEM (9)**

Task and Task states – Task and data – Semaphore and shared data operating system services – Message queues timing functions – Events – Memory management – Interrupt routines in an RTOS environment – Basic design using RTOS.

**UNIT - III EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS (9)**

Custom single purpose processors: Hardware – Combination Sequence – Processor design – RT level design – optimising software: Basic Architecture – Operation – Programmers view – Development Environment – ASIP – Processor Design – Peripherals – Timers, counters and watch dog timers – UART – Pulse width modulator – LCD controllers – Key pad controllers – Stepper motor controllers – A/D converters – Real time clock.

**UNIT - IV MEMORY AND INTERFACING (9)**

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

**UNIT - V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN (9)**

Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology; Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

**Total 45****Reference Books**

- 1 David. E.Simon “An Embedded Software Primer”, Pearson Education, 2001.
- 2 Frank Vahid and Tony Gwargie “Embedded System Design”, John Wiley & sons, 2002.
- 3 Steve Heath, “Embedded System Design”, Elserien, Second Edition, 2004.

**UNIT - I FUNDAMENTALS OF COMPUTER DESIGN (9)**

Review of fundamentals of CPU, Memory and IO – Performance evaluation – Instruction set principles – Design issues – Example Architectures.

**UNIT - II INSTRUCTION LEVEL PARALLELISM (9)**

Pipelining and handling hazards – Dynamic Scheduling – Dynamic hardware prediction – Multiple issue – Hardware based speculation – Limitations of ILP – Case studies.

**UNIT - III INSTRUCTION LEVEL PARALLELISM WITH SOFTWARE APPROACHES (9)**

Compiler techniques for exposing ILP – Static branch prediction – VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism - Hardware versus software speculation mechanisms – IA 64 and Itanium processor.

**UNIT - IV MEMORY AND I/O (9)**

Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.

**UNIT - V MULTIPROCESSORS AND THREAD LEVEL PARALLELISM (9)**

Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Multithreading.

**Total 45****Reference Books**

- 1 John L.Hennessey and David A.Patterson, "Computer Architecture: A Quantitative Approach", Third Edition, Morgan Kaufmann, 2003.
- 2 D.Sia, T.Fountain and P.Kacsuk, "Advanced computer Architectures: A Design Space Approach", Addison Wesley, 2000.

**UNIT - I SYMMETRIC CIPHERS (9)**

Overview – classical Encryption Techniques – Block Ciphers and the Data Encryption standard – Introduction to Finite Fields – Advanced Encryption standard – Contemporary Symmetric Ciphers – Confidentiality using Symmetric Encryption.

**UNIT - II PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS (9)**

Introduction to Number Theory – Public-Key Cryptography and RSA – Key Management – Diffie-Hellman Key Exchange – Elliptic Curve Cryptography – Message Authentication and Hash Functions – Hash Algorithms – Digital Signatures and Authentication Protocols.

**UNIT - III NETWORK SECURITY PRACTICE (9)**

Authentication Applications – Kerberos – X.509 Authentication Service – Electronic mail Security – Pretty Good Privacy – S/MIME – IP Security architecture – Authentication Header – Encapsulating Security Payload – Key Management.

**UNIT - IV SYSTEM SECURITY (9)**

Intruders – Intrusion Detection – Password Management – Malicious Software – Firewalls – Firewall Design Principles – Trusted Systems.

**UNIT - V WIRELESS SECURITY (9)**

Introduction to Wireless LAN Security Standards – Wireless LAN Security Factors and Issues.

**Total 45**

**Reference Books**

- 1 William Stallings, "Cryptography And Network Security – Principles and Practices", Pearson Education, 3<sup>rd</sup> Edition, 2003.
- 2 Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
- 3 Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
- 4 Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
- 5 Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3<sup>rd</sup> Edition, Pearson Education, 2003.
- 6 Mai, "Modern Cryptography: Theory and Practice", First Edition, Pearson Education, 2003.

## EES E04 MULTIMEDIA SYSTEMS

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### UNIT - I MULTIMEDIA (9)

Introduction – Multimedia modalities, Channels and Medium – Interaction – Communicative Interaction – Objects and Agents – Channels of Communication – Artificial Languages – Natural Communication – Meta-languages – Components of Interactive Multimedia Systems.

### UNIT - II KNOWLEDGE AND USER UNDERSTANDING (9)

Knowledge – Basic idea of knowledge – A working definition – Knowledge representation – Knowledge Elicitation – Know about user applying user knowledge – acquiring user knowledge – User profiling – User modelling.

### UNIT - III INTERACTION, INTERFACE & SEMIOTICS (9)

Traditional HCI – Modalities and the interface – Interface channels – Functionality and usability – Visual appearance and Graphic design – Multimedia content – Semiotics – Idea of a Sign – Complex Signs – Semiotics and Media.

### UNIT - IV TEXT AND SOUND (9)

Visual Perception of Text – Images on Page – Meaning and Text Readability – Text and the Screen – Modality of Sound – Channels of Communication – Combining Sound Channels – Technology of Sound – MIDI.

### UNIT - V IMAGES (9)

Psychology of vision – Representational Images – Juxtaposition of Images – Perception of Motion – Constructing a Shot – Shots into narrative – Modern languages of film and television.

**Total 45**

### Reference Books

- 1 Mark Elsom-Cook, "Principles of Interactive Multimedia" McGraw Hill, International Edition 2001.

**UNIT - I** (9)

Introduction – Operating systems and services – Processes – CPU Scheduling approaches.

**UNIT - II** (9)

Process synchronization – Semaphores – Deadlocks – Handling deadlocks – Multithreading.

**UNIT - III** (9)

Memory management – Paging – Segmentation – Virtual memory – Demand paging – Replacement algorithms.

**UNIT - IV** (9)

Disk Scheduling approaches – File systems – Design issues – User interfaces to file systems – I / O device management.

**UNIT - V** (9)

Case study – Design and implementation of the UNIX OS, process model and Structure – Memory management – File system – UNIX I / O management and Device drivers – Windows – System components – Process management – Memory management – File systems – Networking.

**Total 45**

**Reference Books**

- 1 Abraham Silberschatz Peter B. Galvin, G.Gagne, "Operating System Concepts", 6<sup>th</sup> Edition, Wesley Publishing company, 2003.
- 2 M.J.Bach, Design of the UNIX Operating System, Prentice Hall, 1986.

**UNIT - I VHDL FUNDAMENTALS (9)**

Fundamental Concepts – Modeling Digital Systems – Domains and Levels of Modeling – Modeling Languages – VHDL Modeling concepts – Scalar Data Types and Operations – Constants and variables – Scalar Types – Type Classification – Attributes and Scalar types – Expressions and operators – Sequential Statements – If statements – Case statements – Null Statements – Loop statements – Assertion and Report statements.

**UNIT - II COMPOSITE DATA TYPES & BASIC MODELING CONSTRUCTS (9)**

Arrays – Unconstrained Array types – Array Operations and Referencing – Records – Basic Modeling Constructs – Entity Declarations – Architecture Bodies – Behavioral Descriptions – Structural Descriptions – Design Processing.

**Case Study:** A pipelined Multiplier Accumulator.

**UNIT - III SUBPROGRAMS AND PACKAGES (9)**

Procedures – Procedure Parameters – Concurrent Procedure Call Statements – functions – Overloading – Visibility of Declarations – Packages and Use Clauses – Package declarations – Package bodies – Use Clauses – The predefined – Aliases – Aliases for data objects – Aliases for Non-Data Items.

**Case Study:** A Bit-Vector Arithmetic Package.

**UNIT - IV SIGNALS, COMPONENTS, CONFIGURATIONS (9)**

Basic Resolved signals – IEEE Std\_Logic\_1164 Resolved subtypes – Resolved signal parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – Components and Configurations – Components – Configuring component Instances – Configuration Specification – Generate Statements – generating iterative structure – Conditionally generating structures – Configuration of generate Statements. **Case Study:** The DLX Computer System.

**UNIT - V ADTs AND FILES (9)**

Access Types – Linked Data structures – Abstract Data Types using Packages – Files and Input/Output – Files – The Package Textio – Verilog.

**Case Study:** Queuing Networks.

**Total 45**

**Reference Books**

- 1 Peter J.Ashenden, The Designer's Guide to VHDL, Morgan Kaufmann Publishers, San Francisco, Second Edition, May 2001.
- 2 Zainalabedin Navabi, VHDL Analysis and Modeling of Digital Systems, McGraw Hill International Editions, Second Edition, 1998.
- 3 James M.Lee, Verilog Quick start, Kluwer Academic Publishers, Second Edition, 1999.

## EES E07 WIRELESS AND MOBILE COMMUNICATION

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### UNIT - I INTRODUCTION (9)

Wireless Transmission-signal propagation-spread spectrum-Satellite Networks-Capacity Allocation-FAMA-DAMA-MAC

### UNIT - II MOBILE NETWORKS (9)

Cellular Wireless Networks-GSM-Architecture-Protocols-Connection Establishment-Frequently Allocation-Routing-Handover-Security-GPRA

### UNIT - III WIRELESS NETWORKS (9)

Wireless LAN-IEEE 802.11 Standard-Architecture-Services-Ad.Hoc Network-HiperLan-Blue Tooth

### UNIT - IV ROUTING (9)

Mobile IP-DHCP- AdHoc Networks-Proactive and Reactive Routing Protocols-Multicast Routing

### UNIT - V TRANSPORT AND APPLICATION LAYERS (9)

TCP over Adhoc Networks-WAP-Architecture-WWW Programming Model-WDP-WTLS-WTP-WSP-WAE-WTA Architecture-WML-WML scripts.

**Total 45**

### Reference Books

- 1 Kaveh Pahlavan, Prasanth Krishnamoorthy, " Principles of Wireless Networks' PHI/Pearson Education, 2003
- 2 Uwe Hansmann, Lothar Merk, Martin S. Nicklons and Thomas Stober, " Principles of Mobile computing", Springer, New york, 2003.
- 3 C.K.Toth, " AdHoc mobile wireless networks", Prentice Hall, Inc, 2002.
- 4 Charles E. Perkins, " Adhoc Networking", Addison-Wesley, 2001.
- 5 Jochen Schiller, " Mobile communications", PHI/Pearson Education, Second Edition, 2003.
- 6 William Stallings, " Wireless communications and Networks", PHI/Pearson Education, 2002.